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02/05/02



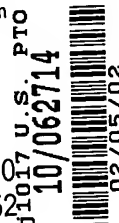
11059 U.S. PTO

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February 5, 2002

ATTORNEY DOCKET NO. 06720.0070  
CUSTOMER NUMBER: 22,852



**Box PATENT APPLICATION**  
Assistant Commissioner for Patents  
Washington, D.C. 20231

Re: New U.S. Patent Application  
Title: SCR DEVICES IN SILICON-ON-INSULATOR  
CMOS PROCESS FOR ON-CHIP ESD PROTECTION  
Inventor(s): MING-DOU KER ET AL.

FEE VALUE ACCOUNTABILITY	
DEPOSIT ACCOUNT NO.	
0610916	
FEE CODE	VALUE FURNISHED

Sir:

We enclose the following papers for filing in the United States Patent and Trademark Office in connection with the above patent application.

1. Application - 26 pages, including 3 independent claims and 35 claims total.
2. Drawings - 10 sheets of formal drawings (Figures 1-8B).
3. Declaration/Power of Attorney.
4. ✓ Recordation Form Cover Sheet - Assignment to Industrial Technology Research Institute

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The filing fee is calculated as follows:

Basic Application Filing Fee					\$740	\$ 740.00
	Number of Claims		Basic	Extra Claims		
Total Claims	35	-	20	15	x \$18	270.00
Independent Claims	3	-	3		x \$84	
[ ] Presentation of Multiple Dep. Claim (s)					+\$270	
					Subtotal	\$ 1010.00
					Reduction by 1/2 if small entity	-
					TOTAL APPLICATION FILING FEE	\$ 1010.

3. A check for \$1050.00 is enclosed. The fee includes:

\$ 740.00 filing fee;  
\$ 270.00 additional claim fee;  
\$ 40.00 Recordation Fee

Please address all correspondence with respect to this application to:

Finnegan, Henderson, Farabow,  
Garrett & Dunner, L.L.P.  
1300 I Street, N.W.  
Washington, D.C. 20005-3315

Please accord this application a serial number and filing date.

Assistant Commissioner for Patents  
February 5, 2002  
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The Commissioner is hereby authorized to charge any additional filing fees due and any other fees due under 37 C.F.R. § 1.16 or § 1.17 during the pendency of this application to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,  
GARRETT & DUNNER, L.L.P.

By: 

Yitai Hu

Reg. No. 40,653

YH:pwl  
Enclosures